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Version History

Date	Version	Description of change	Author
2023-01-04	V1.00	Original	Yaling. Wang

No	Check Items	
1	General inspection	
2	Power supply	VBAT_BB (Pin V45,V49,U47) VBAT_RF (Pin Y49,AC47,AA47, W47,AD45,AB45,Y45)
		VDD_EXT (Pin AL5)
		GND (Pin AH45,AG47,AF45, AE47,AD49,AB49.AA51, W51,U51,T49,R47)
		PWRKEY (Pin A45)

3	Start-up circuit	
		CHG_SYS_OK (Pin C43)
		PON_1
4	RESIN_N circuit	RESIN_N (Pin A43)
5	USB interface	USB_VBUS (Pin C9)
		USB3.0/1 (Pin A13,B14,B10,A9)
		USB_SS_SW (Pin C13)
		USB2.0 (Pin B6,A5)

6		Connector
		OTG function
		USB_ID (Pin C11)
		OTG_EN (Pin D10)
	PCIE interface	PCIE (Pin B22,A21, B18,A17,B20,A19, A25,B26,A23,B24)
		PCIE_WAKE (Pin C25)
		PCIE_RST (Pin C23)
		PCIE_CLKREQ (Pin C21)
		Level shift
	PCIE模块和AP指示状态 信号	SDX2AP_STATUS (Pin T7)
		AP2SDX_STATUS (Pin V7)
		SDX2AP_EP11_STATUS (Pin AG5)
		SDX2AP_ERR_FATAL (Pin U5)
		AP2SDX2_ERR_FATAL (Pin R5)
		WAKE_UP_IN (Pin AE5)

7	W82/W80 interface	WL_VDD_VM (Pin M45)
		WL_VDD_VL (Pin P49)
		WL_VDD_VH (Pin N47)
		Coexistence signal (When the 5G module and the WIFI module share the antenna and the isolation is not higher than 15dB, the coexistence signal needs to be used; when the 5G module and the WIFI module do not share the antenna and the isolation is higher than 15dB, the coexistence signal does not need to be used)
		SLEEP_CLK
		Other control WIFI/BTsignals
8	SD/SDIO interface	SDIO_VDD (Pin F7)
		SD card VDD

		Connect SD card
		Connect eMMC
9	RGMI interface	RGMI_PWR_IN (Pin D32)
		RGMI_PWR_EN (Pin D36)
		RGMI_3P3_EN (Pin D38)
		RGMI_RX (Pin A35,B36, B40,A37,B38,A39) RGMI_TX (Pin A33,B34, A31,B30,A29,B32)
10	EBI interface interface	EBI interface

11	UART interface	UART interface
12	I2C circuit	I2C circuit
13	Audio interface	I2S/PCM
14	SPI interface	SPI

15	(U)SIM card interface	(U)SIM_VDD
		(U)SIM card interface
16	GPIO	GPIO usage check
		PIN with boot function

17	Force download circuit FORCED_USB_BOOT	USB_BOOT (Pin D12)
18	RF circuit	RF circuit
		mmW circuit

19	PMI interface	L10E_3P1 (Pin C41)
		VIO_OUT (Pin D42)
		SPMI_CLK(Pin A47) SPMI_DATA(Pin B46)
		FAULT_N (Pin B44)
		CHG_SYS_OK (Pin C43)
20	PM7250B circuit	VBATT_SNS
		BATT_ID
		NTC
		VPH_PWR
		USB_DP/DM
		CC
		TYPEC_VBUS_IN

315/X55/X65/X62 Series 5G LGA Module Schematic Check List

Detailed check contents
Confirm whether the module schematic symbols provided by SIMCom are used. If the customer designs the symbol by himself, make sure that the symbol is correct.
If the function of the GPIOs used by the customer is inconsistent with the default of SIMCom, the application information of these GPIOs should be provided to SIMCom for inspection.
Module main power input. The voltage range is 3.3V~4.4V, the typical voltage is 3.8V, and the continuous supply current is at least 3A.
It is recommended that the module use a dedicated DC/DC switching regulators, which is not shared with other loads. If the VBAT network is connected to other DC/DC switching regulators inputs, it is recommended to use magnetic beads to separate the VBAT network from other DC/DC switching regulators input to reduce interference.
The total capacitance value of the capacitor placed near the VBAT pin of the module shall be greater than 640uF to ensure that when the module VBAT is at 3.8V and the maximum power consumption, the input voltage is not lower than 3.3V after an instantaneous (ms level) drop.
In addition to parallel high value capacitors, incorporate a group of small capacitors into VBAT_BB and VBAT_RF respectively to filter out high-frequency interference, and at least reserve space for components during design. (1uF+100nF+100pF+33pF combination is recommended)
In order to improve the ESD and surge protection capability of the module, it is recommended to use a TVS whose Vrwm is 4.8V or 5V. The clamping voltage should be as close as possible to the input voltage of the module, while ensuring that Ipp is high enough. For example, TVS WS4.5DPV, when VC=7V, IPP=80A.
If the motherboard uses a DC adapter to cooperate with the power conversion circuit to supply power to the module, TVS must be used at the interface of the DC adapter, and Vrwm is not lower than the maximum output voltage of the DC adapter.
1.8V power output. It is mainly used as the power supply for pulling up the module pin, and the maximum output current is 50mA.
The total capacitance in parallel with this pin should be less than 2.2uF.
It is recommended to connect a 0R resistor in series close to VDD_EXT, then connect TVS (Vrwm: 2.5~3V) in parallel and then connect the load. To further improve the ESD protection capability of this pin, replace the 0R resistor with 2.2R. This pin is very sensitive to static electricity and surge, please pay attention to protection. (The module using the X65 platform has already connected TVS in parallel to this pin, which has a certain ESD protection capability, and usually does not need to add TVS) When using VDD_EXT to supply power to the VDD_IO of the W82/W80 WIFI module, the resistance in series in the middle must be 0R to prevent the resistance from dividing the voltage, resulting in IO levels that do not meet the requirements of electrical characteristics.
These pins are VBAT return paths, all of which should be used and placed with enough ground via.
Power on/off signal input, active low. When the module is in the power-off state and the PWRKEY pull-down time is longer than 0.4s, the module will be turned on; when the module is in the power-on state and the PWRKEY pull-down time is longer than 2s, the module will be turned off. When the module VBAT is powered on, the PWRKEY voltage is 1.1V, pay attention to level matching when using it.
If physical buttons are used to turn on or off the module, the buttons should be connected in parallel with TVS, and the junction capacitance of TVS should be less than 10pF.
It is not recommended to use the RC circuit to power on. It is recommended to use MCU GPIO and NPN triode to control the PWRKEY to realize booting (as shown in the right figure).

It is forbidden to continuously pull down PWRKEY to achieve power-on and start-up. In this way, the module will restart repeatedly.
<p>If the PM7250B charging chip is not used, CHG_SYS_OK can be continuously pulled down to realize the function of automatically turning on when the power is supplied. This pin is forbidden to be used with PWRKEY (Pin A45) at the same time.</p> <p>(Only modules using the X65/X62 platform support this function)</p>
<p>If you need the module to start automatically when it is powered on, you can keep pulling this pin high. This pin is forbidden to be used with PWRKEY (Pin A45) at the same time.</p> <p>(Only modules using the X55/X315 platform support this function)</p>
Reset signal input, active low. The working voltage of RESIN_N is 1.8V, pay attention to level matching when designing.
If physical buttons are used to reset the module, the buttons should be connected in parallel with TVS.
It is recommended to use MCU GPIO and NPN transistor to control RESIN_N to reset module (Reference PWRKEY circuit).
It is recommended to connect a 10nF capacitor in parallel to the RESIN_N pin to prevent crosstalk from causing reset.
VBUS detection pin of USB interface. When the voltage of USB_VBUS is in the range of 1.8~5.0V, the power supply of USB_PHY 3V1 is turned on inside the module, and the USB interface starts to work normally. USB_VBUS must be externally supplied with 1.8~5.0V voltage, otherwise the USB interface will not work normally
The USB_SS_RX_P/M and USB_SS_TX_P/M differential pairs must adopt 85 ohm differential impedance control, and the difference between the lengths of the two traces of the differential pair should be less than 0.5mm. These requirements should be marked on the schematic diagram. If USB_SS is connected to a USB connector (such as Type-C, etc.), TVS must be connected in parallel close to the connector to provide ESD protection, and the TVS junction capacitance must be less than 0.5pF.
<p>The USB_SS signal requires an AC capacitor connected in series between the transmitter and receiver for AC coupling, and the capacitor should be as close to the transmitter as possible. USB_SS_TX_P/M has a pair of 220nF AC capacitors connected in series inside the module, no external capacitors are needed;</p> <p>If the USB_SS_RX_P/M is directly connected to the IPQ or AP chip, a 220nF AC capacitor needs to be connected in series near the IPQ or AP end.</p>
<p>Notice:</p> <p>When connected to the USB female connector, connect USB_SS_TX to TX, and USB_SS_RX to RX (because the Type-C/A cable internally crosses TX and RX).</p> <p>When connecting a USB male connector and a chip such as IPQ or AP, USB_SS_TX is connected to RX, and USB_SS_RX is connected to TX.</p> <p>Please confirm the differential pair between the module and the peer device (module, chip, connector, etc.), P is connected to P, and N is connected to N.</p>
When the customer does not use the PM7250B charging chip, but needs the USB3.0 Type-C positive and negative insertion function, USB_SS_SW can be used to switch the channel of the USB_SS signal switch chip. (See reference design for details)
<p>The USB_HS_DP/M differential pair must adopt 90 ohm differential impedance control, and the difference between the lengths of the two traces of the differential pair should be less than 0.7mm. These requirements should be marked on the schematic diagram. If USB_HS is connected to a USB connector (such as Type-C, etc.), it is recommended to connect the common mode inductor (DLW21SN670SQ2L, MURATA) in series close to the connector to improve the common mode noise rejection capability. Confirm whether the module has a built-in TVS, if not, a TVS must be connected in parallel between the common-mode inductor and the USB connector. The TVS junction capacitance must be less than 0.5pF.</p> <p>If the USB_HS_DP/M is connected to the AP chip, it is recommended to connect a 0 ohm resistor in series for easy commissioning.</p> <p>Please confirm the differential pair between the module and the peer device (module, chip, connector, etc.), P is connected to P, and N is connected to N.</p> <p>(The USB2.0 interface must be drawn out for forced firmware update)</p>

If use Mirco-USB or Type-C connector, must ensure that the connector pin definition and PCB package are correct.
When the module is in master mode and provides OTG function, it is necessary to increase the peripheral circuit to provide 5V power supply to the slave device. (see reference design for details)
Signal input, effective at low voltage. When USB_ID is pulled down, the module is in master mode. Mirco-USB interface, inserting a U disk and other slave devices USB_ID is pulled down. For the Type-C interface, an additional CC chip is required to control the USB_ID to be pulled down.
When USB_ID is pulled down, USB_OTG_EN outputs high level to control OTG 5.0V power output.
Support 2 lane PCIE3.0, 8Gbps per lane, backward compatible with PCIE2.0 and PCIE1.0.
PCIE_RX0_P/M, PCIE_RX1_P/M, PCIE_TX0_P/M, PCIE_TX1_P/M, PCIE_REFCLK_P/M differential pairs must adopt 85 ohm differential impedance control, and the difference between the lengths of the two traces in the differential pair should be less than 0.5mm. These requirements should be specified Identified in the
The PCIE signal needs to be AC-coupled by connecting an AC capacitor in series between the transmitter and the receiver, and the capacitor should be as close as possible to the transmitter. PCIE_TX0_P/M, PCIE_TX1_P/M have connected 220nF AC capacitor in series inside the module, no external capacitor is needed. PCIE_RX0_P/M and PCIE_RX1_P/M must be connected in series with a 220nF AC capacitor at the opposite chip pin of the module.
This pin is signal input when the module is in RC mode. This pin is a signal output when the module is in EP mode. 1.8V level, pay attention to level matching when designing, and must be pulled up to VDD_EXT through a 10K resistor.
This pin is signal output when the module is in RC mode. This pin is a signal input when the module is in EP mode. 1.8V level, pay attention to level matching when designing.
This pin is signal input when the module is in RC mode. This pin is a signal output when the module is in EP mode. 1.8V level, pay attention to level matching when designing, and must be pulled up to VDD_EXT through a 10K resistor.
There is no 1.8V to 3.3V level conversion chip inside the module. If it needs to be connected to a 3.3V PCIE interface, a peripheral circuit for level conversion should be designed. If you are not sure whether the pins of the level conversion chip used are internally pulled up, it is recommended to reserve pull-up resistors at both ends. Note: When the following conditions exist at the same time, the computer cannot be shut down. 1. The enable pin of the LDO is controlled by VDD_EXT and the LDO has an output discharge function. When the computer is turned off, VDD_EXT stops outputting, the output of LDO is short-circuited to GND, and the PCIE_WAKE signal is forcibly pulled down by the output of LDO. 2. When PCIE_WAKE is at low level, the computer system mistakenly believes that the module is still transmitting data, and will restart the computer.
If NMOS is used to implement level conversion, the level of G should be consistent with that of S.(as shown in the right figure)
Signal output. When the module is turned on normally and successfully registered with the network, this pin outputs a high level to the AP. When the module is turned on or registered with the network abnormally, this pin outputs a low level to the AP.
Signal input. When the AP is turned on normally, this pin outputs a high level to the module. When the AP is turned on abnormally, this pin outputs a low level to the module.
Signal output. When the module can make an emergency call, this pin outputs a high level to the AP.
Signal output. When the module has a fatal error, this pin outputs high level to the AP.
Signal input. When the AP has a fatal error, this pin outputs high level to the module.
signal input. When the module sleeps, pull this pin low to wake up the module.

Power Output. The maximum output current is 0.6A, only for SIMCom W82/W80 WIFI module.
WL_VDD_VM should be connected in parallel with 10uF+1uF+100nF capacitor.
Power Output. The maximum output current is 1.7A, only for SIMCom W82/W80 WIFI module.
WL_VDD_VL should be connected in parallel with 10uF+1uF+100nF capacitor.
Power Output. The maximum output current is 0.6A, only for SIMCom W82/W80 WIFI module and mmW QTM antenna module.
WL_VDD_VH should be connected in parallel with 10uF+1uF+100nF capacitor.(When used for WIFI module)
The COEX_UART_TXD (Pin BA7), COEX_UART_RXD (Pin BA9) serial port signals are the coexistence signals of the LTE frequency band of the module and the 2.4G frequency band of the WIFI module. Pay attention to the signal direction when designing.
The output signal of WL_LAA_TX_EN (Pin R51) and the input signal of WL_TX_EN (Pin AY14) are the coexistence signals of the LAA frequency band of the module and the 5G frequency band of the WIFI module. Pay attention to the signal direction when designing. Note: SIM8260C/E/A, SIM8360E/A do not use WL_LAA_TX_EN, please keep floating. SIM8260C does not use WL_TX_EN, please keep floating.
The N79_TO_WL_TXEN (Pin BA29) output signal and the WL_TXEN_TO_N79 (Pin BA37) input signal are the coexistence signals of the N79 frequency band of the module and the W82 WIFI module. Pay attention to the signal direction when designing. Note: Modules using the X55/315 platform do not support the definition of these two pins. SIM8260C/E/A, SIM8360E/A do not use N79_TO_WL_TXEN, please keep it open.
32KHz sleep clock output, connected to WIFI module.
BT_EN(Pin N51), WL_EN(Pin K45), WL_LAA_RX(Pin J47), WL_LAA_AS_EN(Pin L51), WL_PA_MUTING(Pin H45) are the control signals of W80/W82 WIFI module and 5G module. If the WIFI module does not have functions such as LAA or BT, these pins can be pulled down through a 10K resistor on the W80/W82 WIFI module side. (For more information, please refer to the Hardware Design Guide) These pins can be configured as GPIOs if the W82 is not used.
For other control signal design principles, please refer to the hardware design guidelines and reference designs.
Power input. For pull up SDIO VDD_IO. Ensure that the supply current is at least 50mA. When SDIO is connected to SD card, it is necessary to provide 1.8V or 2.85V switchable dual power supply for this pin to adapt to SD cards with different voltages; When SDIO is connected to EMMC, it is necessary to provide 1.8V power supply for this pin; When SDIO is not used, this pin needs to be connected to VDD_EXT.
1uF capacitor should be connected in parallel close to the SDIO_VDD pin.
The SD card needs an external circuit to provide a 2.95V power supply. If it needs to support SD3.0, the current consumption can reach 0.8A or even higher. Therefore, the power supply current of the external circuit should be designed according to the datasheet of the SD card used.
A 10K resistor for pulling up to SDIO_VDD (Pin F7) is reserved for SD_DATA [0:7] and SDC_CMD signals, which are not assembled by default. When SDIO is connected to 8-wire EMMC, it is recommended to connect the 0R resistor in series. The connection relationship is as follows: SDIO_VDD_EN (Pin H7) is connected to EMMC_DATA4. SDIO_DET (Pin E1) is connected to EMMC_DATA5. GPIO100 (Pin H3) is connected to EMMC_DATA6. GPIO101 (Pin K7) is connected to EMMC_DATA7.
The pins of the SD card socket should be connected in parallel with ESD protection devices such as TVS, and the parasitic capacitance should be less than 2pF as much as possible. Excessive capacitance will affect the reading and writing speed of the TF card, and even lead to failure of reading and writing. SDIO bus load capacitance should be less than 15pF.

<p>Confirm whether the SD card socket supports hot swapping, and whether the detection pin of the socket is at high level or low level after the card is inserted (that is, active low or active high). SDC_DET needs to be pulled up to VDD_EXT (Pin AL5) through a 470K resistor.</p>
<p>The SDIO trace should control 45 ohm single-ended impedance, and mark the impedance requirement on the schematic diagram.</p>
<p>It is recommended to connect a 0R resistor in series with the SDIO_CLK pin. (The module using the X62 platform has already connected a 33R resistor in series with this pin, and there is no need to connect a resistor in series externally)</p>
<p>SD_VDD_EN is used to enable the VDD power supply (2.95V) and SDIO_VDD power supply (1.8/2.85V) of the SD card, active high.</p>
<p>GPIO100 (Pin H3) is used to switch the 1.8V and 2.85V input power of SDIO_VDD (Pin F7). It should be switched to 2.85V when the output is high, and it should be switched to 1.8V when the output is low.</p>
<p>RESOUT_N (Pin AW17) is connected to RESIN_N of eMMC. SDIO_CMD (Pin G5) is connected to CMD of eMMC. SDIO_CLK (Pin E5) is connected to CLK of eMMC. The module does not have a pin connected to R_CLK of EMMC, which can be connected to GND through a 10K resistor on the EMMC chip side.</p>
<p>Power input. Provide power for the IO of the module RGMII interface, the voltage is determined by the IO level of the Ethernet PHY chip, and the module supports 1.8V level by default. 1uF capacitor should be connected in parallel close to the RGMII_PWR_IN pin. When the RGMII interface is not used, this pin needs to be connected to VDD_EXT.</p>
<p>Signal output. Used to enable the RGMII_PWR_IN power supply.</p>
<p>Signal output. Used to enable the RGMII_PWR_3V3 power supply for the Ethernet PHY chip.</p>
<p>Check whether the relationship between the RGMII_RX/RGMII_TX signal and the peripheral connection is correct, and pay attention to the direction of the signal. (Note that the output pin name of some PHY chips is RX, and the input pin name is TX).</p>
<p>The RGMII_RX and RGMII_TX traces should control 50 ohm single-ended impedance, and the length difference between the signals in the RGMII_RX or RGMII_TX group should not exceed 5mm.</p>
<p>The level of RGMII_RST_N (Pin C29) is 1.8V. Active low. Pay attention to level matching when designing. The timing can be controlled by RC circuit or GPIO. For more information, refer to the Hardware Design Guide. The level of RGMII_INT_N (Pin C39) is 1.8V. Active low. Pay attention to level matching when designing.</p>
<p>It is recommended to reserve 0R (or 22R) series resistors on each pin of RGMII_TX/TX_CLK/TX_CTL, RGMII_RX/RX_CLK/RX_CTL, and place them close to the signal output terminals of the module and PHY chip.</p>
<p>RGMII_MD_CLK (Pin D34), RGMII_MD_IO (Pin D30) must be used, and RGMII_MD_IO should be pulled up through a 4.7K resistor (the MD_IO/MD_CLK pin of AR8035 is in the 2.5V voltage domain, pay attention to level matching when designing). The EN pin of the level conversion chip must be active high, such as controlled by VDD_EXT.</p>
<p>Verify that the EBI2_AD[0:7], EBI2_WE_N(Pin A35), EBI2_CLE(Pin A31), EBI2_RE_N(Pin B32), EBI2_CS(Pin AH3) signals are correctly connected with the LCD.</p>
<p>EBI2_AD[0:7], EBI2_WE_N, EBI2_CLE, EBI2_RE_N, EBI2_CS should control 50 ohm single-ended impedance, the trace length difference of each signal should not exceed 5mm, and the trace length should not exceed 100mm.</p>
<p>The highest resolution supports HVGA, 320 (V) × 480 (H) pixels, up to 30 fps; color depth 18 bits/pixel (RGB 6-6-6) or 16 bits/pixel (RGB 5-6-5).</p>
<p>EBI is a 1.8V level interface, pay attention to level matching when using it. The EBI interface is shared with the internal nand of the 5G Module. The EBI interface cannot be used for other purposes except to connect to EBI_LCD.</p>
<p>UART1 is a 7-wire serial port, and can also be used as a 4-wire or 2-wire serial port. By default, UART1_DTR is used to wake up the sleeping module, and it is recommended to connect it.</p>

UART2 is a 4-wire serial port, which is not supported by modules using X65 and X62 platforms, and UART2 of modules using X55/315 platforms cannot be used with BT_UART at the same time.

BT_UART is a 4-wire serial port, which is connected to the W82/W80 Module by default.

DBG_UART_TXD/RXD is only used for system debugging. When the Module is powered on, UART_TXD has log output and cannot be shielded. It is recommended to leave test points or connector interfaces for debugging.

Verify that the UART signal and the peripheral are connected correctly, pay special attention to the direction of the signal

Module UART_TX connects to AP UART_RX

Module UART_RX connects to AP UART_TX

Module UART_CTS connects to AP UART_RTS

Module UART_RTS connects to AP UART_CTS

The UART interface rate is up to 4Mbps, and cannot be used for higher rate requirements, 115200bps is recommended.

UART working level is 1.8V, please pay attention to level matching when designing. The recommended level conversion is shown in the figure on the right.

When the baud rate of the UART interface is more than 460Kbps, it is not recommended to use transistors for level conversion

I2C working level is 1.8V, please pay attention to level matching when designing.

If it is connected to a level conversion chip, make sure that the chip meets the I2C transmission rate requirements.

If you are not sure whether the pull-up resistor is integrated inside the level conversion chip used, it is recommended to reserve pull-up resistors on both sides of it.

Confirm whether the value of the pull-up resistor meets the requirements of the communication rate. Generally, a 2.2K pull-up resistor is recommended.

The device address on the same group of I2C cannot be the same .

Verify that the I2S/PCM signal and the peripheral are connected correctly, pay special attention to the direction of the signal.

By default, the module supports two I2S interfaces with 48KHz sampling rate and 16-bit sampling depth.

I2S is used to connect to the audio CODEC chip by default, and BT_I2S is used to connect to the W82 module by default. (Modules using the X55/315 platform do not support BT_I2S).

If the audio CODEC chip used is not recommended by SIMCom, please contact SIMCom for evaluation.

Verify that the SPI signal and the peripheral are connected correctly, pay special attention to the direction of the signal

The SPI interface of the module only supports master mode, and the rate is up to 50MHz.

SPI is used by default to support LCD with SPI interface or to connect LE9643 chip to expand VOIP function (the software of the standard version module does not support it).

1.8/3.0V dual voltage self-adaptive output, suitable for (U)SIM cards with different voltages.

Note that the load capacitors of (U)SIM1_VDD(Pin B51) and (U)SIM2_VDD(Pin F49) have a capacitance range of 100nF-470nF and should be placed close to the (U)SIM card socket (220nF+33pF is recommended).

<p>Confirm the load capacitance of the (U)SIM signal (parallel capacitance, TVS parasitic capacitance, series resistance, etc.), and test the rising edge Tr and falling edge Tf of (U)SIM_CLK. (U)SIM_CLK: Tr<50ns Tf<50ns.</p> <p>The initial voltage of (U)SIM_VDD is 1.8V. When the (U)SIM card is detected, if the waveform of (U)SIM_CLK is bad, the (U)SIM card may not be recognized. The voltage of (U)SIM_VDD will increase to 3V and the card will be recognized again. If the (U)SIM card is inserted at this time is 1.8V, the (U)SIM card must be removed.</p>
<p>(U)SIM1_CLK(Pin D49), (U)SIM1_RST(Pin C51), (U)SIM1_DATA(Pin E51) are connected in series with 22R resistors and reserve 15pF filter capacitors. It is generally recommended that filter capacitors not be assembled, and ensure that the total capacitance (parasitic capacitance and filter capacitor) of CLK and DATA signals is not greater than 30pF.</p>
<p>(U)SIM2_CLK(Pin H49), (U)SIM2_RST(Pin G51), (U)SIM2_DATA(Pin G47) are connected in series with 22R resistors and reserve 15pF filter capacitors. It is generally recommended that filter capacitors not be assembled, and ensure that the total capacitance (parasitic capacitance and filter capacitor) of CLK and DATA signals is not greater than 30pF.</p>
<p>(U)SIM_DATA has been pulled up to (U)SIM_VDD through a 20K ohm resistor inside the module. The peripheral circuit of the module should reserve the 10K pull-up resistor that is not assembled.</p>
<p>(U)SIM1_DET(Pin E47), (U)SIM2_DET(Pin F45) are used for (U)SIM card hot plug detection. To use the hot-swap function, these two pins should be pulled up to VDD_EXT through a 100K resistor.</p> <p>The software default configuration, when the (U)SIM card is not inserted, (U)SIM_DET and GND are short-circuited, after the (U)SIM card is inserted, (U)SIM_DET and GND are open, and (U)SIM_DET changes from low level to high level, that is, the rising edge Valid (you can use the AT+UIMHOTSWAPLEVEL=0 or 1 command to change this logic to adapt to different (U)SIM card sockets).</p> <p>The hot swap function is disabled by default in the software (you can use the AT+UIMHOTSWAPON=1,1 command to enable the card slot 1 hot swap function; you can use the AT+UIMHOTSWAPON=1,2 command to enable the card slot 2 hot swap function).</p>
<p>All pins of the (U)SIM card socket need to add TVS to ensure ESD protection capability (the junction capacitance of the ESD protection component should be less than 15pF).</p>
<p>Check the connection relationship between the module and the (U)SIM card socket, and whether the package of the (U)SIM card socket is correct.</p>
<p>GPIO signal level is 1.8V, pay attention to level matching when designing.</p>
<p>If there is a requirement for the ESD protection capability of GPIO, ESD protection devices such as TVS can be added. In addition, on the premise of not affecting the function, it is recommended to connect a 100R resistor in series at the module end to further improve the ESD protection capability.</p>
<p>Pay attention to the leakage problems caused by different voltage domains, such as: whether the power source selected by the pull-up resistor is correct.</p>
<p>If you want to wake up the module, please select the GPIO with the wake-up function of the module. For the specific pin definition, please refer to the module hardware design guide.</p>
<p>For modules using the X62/X65 platform, the pins with the BOOT_CONFIG function are as follows:</p> <p>EBI2_WE_N(Pin A35)-GPIO24</p> <p>EBI2_CLE(Pin A31)-GPIO21</p> <p>USB_BOOT(Pin D12)-GPIO42</p> <p>EBI2_AD_0 (Pin A33)-GPIO50</p> <p>EBI2_AD_1 (Pin A39)-GPIO51</p> <p>EBI2_AD_2 (Pin B34)-GPIO52</p> <p>EBI2_AD_3 (Pin B38)-GPIO54</p> <p>EBI2_AD_4 (Pin C39)-GPIO55</p> <p>EBI2_AD_5 (Pin B36)-GPIO58</p> <p>EBI2_AD_6 (Pin B40)-GPIO59</p> <p>EBI2_AD_7 (Pin A37)-GPIO60</p> <p>BT_UART_RTS (Pin U5)-GPIO66</p> <p>Do not pull up the above pins, otherwise it will affect the power-on of the module.</p>
<p>For modules using the X55/315 platform, the pins with the BOOT_CONFIG function are as follows:</p> <p>BT_UART_TX (Pin K6)-GPIO63</p> <p>USB_BOOT(Pin D12)-GPIO42</p> <p>Do not pull up the above pins, otherwise it will affect the power-on of the module.</p>

USB_BOOT (Pin13) is used for forced download, and a test point needs to be reserved to upgrade the software by pulling it up to 1.8V. It is forbidden to pull up this pin when the module is powered on normally.
The RF circuit requires a π -type matching circuit. The module has a variety of antenna quantity specifications such as 4 antennas, 5 antennas, or 6 antennas. For more information, please refer to the hardware design guide.
The correctness of the antenna matching circuit, tuner circuit, and SAR sensor circuit needs to be confirmed with the RF engineer.
The RF frequency band, CA combination, and antenna frequency band allocation supported by the module need to be confirmed with the RF engineer.
ANT_CTRL0, ANT_CTRL1, RFFE0_DATA, and RFFE0_CLK are used by default for the antenna tuner, and it is not recommended to use them for other purposes.
If ESD protection design is considered, TVS can be used, and the TVS junction capacitance should be less than 0.05pF. (To avoid affecting RF performance, it is recommended that TVS is not assembled by default)
The signal connection relationship between the module using the X65 platform and the QTM545/547 module is as follows: VREG_1P9(Pin N47) IFV4(Pin AP45)、IFH3(Pin AL51)、QTM0_PON(Pin AT49)接QTM U1; IFV2(Pin AT45)、IFH1(Pin AR51)、QTM1_PON(Pin AH49)接QTM U2; IFV3(Pin AK45)、IFH4(Pin AC51)、QTM2_PON(Pin AF49)接QTM U3; IFV1(Pin AM45)、IFH2(Pin AG51)、QTM3_PON(Pin AP49)接QTM U4。
The signal connection relationship between the module using the X55 platform and the QTM525 module is as follows: VREG_1P9(Pin N47) IFV4(Pin AM45)、IFH1(Pin AG51)、QTM0_PON(Pin AT49)接QTM U1; IFV1(Pin AT45)、IFH4(Pin AR51)、QTM1_PON(Pin AH49)接QTM U2; IFV3(Pin AK45)、IFH2(Pin AC51)、QTM2_PON(Pin AF49)接QTM U3; IFV2(Pin AP45)、IFH3(Pin AL51)、QTM3_PON(Pin AP49)接QTM U4。
The signal connection relationship between the module using the X55 platform and the QTM527 module is as follows: VREG_1P9(Pin N47) IFV4(Pin AM45)、IFH1(Pin AG51)、QTM3_PON(Pin AP49)接QTM U1; IFV3(Pin AK45)、IFH2(Pin AC51)、QTM0_PON(Pin AT49)接QTM U2; IFV2(Pin AP45)、IFH3(Pin AL51)、QTM1_PON(Pin AH49)接QTM U3; IFV1(Pin AT45)、IFH4(Pin AR51)、QTM2_PON(Pin AF49)接QTM U4。
QTM_THERM (Pin AW19) is used for QTM module by default, and it is not recommended to use it for other purposes.
WL_VDD_VH (1.9V) needs to add 4.7uF+22pF filter capacitor (mmW). The current of a single QTM module is greater than 0.2A, and the DC ESR of the power trace is less than 100m Ω . (Only one QTM545 module works at the same time, and four QTM547 modules can work together at the same time)
VBAT needs to add 10uF+100pF filter capacitor (mmW). The current of a single QTM module is greater than 1.5A, and the DC ESR of the power trace is less than 80m Ω . (Only one QTM545 module works at the same time, and four QTM547 modules can work together at the same time)
A 47uF~100uF capacitor is reserved near the main power supply pin of the QTM module to prevent voltage instability. It is not assembled by default.
The model of the board-to-board male connector used on the QTM545 module is AXG4B0612DJ1/818019183, and the model of the mated board-to-board female connector is AXG3B0612DJ1/818022986. Please pay attention to whether the model is selected correctly.
Module power output. When USB_VBUS is 1.8~5.0V, L10E_3P1 supplies power to the outside. This pin is only used for power supply of PM7250B charging chip, USB_SS switch chip and CC chip.
A 1uF capacitor should be connected in parallel close to the L10E_3P1 pin.

<p>By default, the VDD power supply of the CC chip is provided by L10E_3P1. When not connected to the computer, the power supply of the CC chip is turned off.</p> <p>If VDD of the CC chip is supplied with a 3.3V power supply by the peripheral circuit, when the USB cable is inserted, the CC voltage in the USB cable will become 3.3V, because there is a 56K ohm resistor between CC and VBUS in the cable, which will cause the USB_VBUS voltage to be higher than 1.8 V, so the module mistakenly thinks it is connected to the computer and adjusts to USB virtual port mode. Therefore, the USB_VBUS should be pulled down to GND through a 5.6K ohm resistor to ensure that the USB_VBUS voltage is lower than 1.8V.</p>
<p>Module power output. When the VBAT of the module is powered on, this pin outputs 1.8V power, which is only used for the PM7250B charging chip.</p>
<p>A 1uF capacitor should be connected in parallel close to the VIO_OUT pin.</p>
<p>SPMI_CLK and SPMI_DATA should be connected in series with 0R resistors for easy debugging. The SPMI_CLK and SPMI_DATA traces should control 50 ohm single-ended impedance and be isolated with stitched ground on both sides.</p>
<p>PM_FAULT_N should be connected in series with 0R resistors for easy debugging and be isolated with stitched ground on both sides.</p>
<p>When the PM7250B charging chip is working, CHG_SYS_OK outputs a low level, which is used to control the module to start. CHG_SYS_OK should be connected in series with a 0R resistor for debugging.</p>
<p>VBATT_SNS_P and VBATT_SNS_M are voltage detection signal inputs. These pins cannot be left floating and series resistors are not recommended to avoid affecting measurement accuracy. VBATT_SNS_P and VBATT_SNS_M should be directly connected to the battery connector, should be routed on the inner layer and be isolated with stitched ground on both sides.</p>
<p>BATT_ID is the battery presence detection pin, which cannot be left floating. Do not connect capacitors in parallel to this signal. When the battery has an ID interface, connect to the battery ID interface. When the battery has no ID interface or the motherboard is powered by an adapter, pull it down to GND through a 100K resistor.</p>
<p>BATT_THERM is used to measure the battery temperature and cannot be left floating. Do not connect capacitors in parallel to this signal. When the battery has a THERM interface, connect to the battery THERM interface. When the battery has no BATT_THERM interface or the motherboard is powered by an adapter, pull it down to GND through a 100K resistor.</p> <p>In order to ensure the stability of measuring battery temperature, please note:</p> <ol style="list-style-type: none"> 1. Do not assemble the battery NTC resistor on the battery protection board. It is recommended to use a lead-type tadpole-shaped NTC resistor to avoid the temperature interference of the protection board; 2. The NTC resistor avoid sharing the return path with the battery power supply. It should be directly connected to the module with a separate trace, and the battery uses a separate pin to connect to the GND pin of the NTC resistor.
<p>CONN_THERM is used to measure the temperature of the Type-C connector. A 100K NTC resistor should be placed close to the Type-C connector and away from heat sources.</p>
<p>AMUX_1 is used to measure the temperature of the PM7250B charging chip, and a 100K NTC resistor needs to be placed close to the PM7250B chip.</p>
<p>VPH_PWR is the power output of PM7250B charging chip, the voltage range is the same as VBAT, and the maximum output current is 4A. If the PM7250B charging chip is used, the module needs to obtain power from here, otherwise the fuel gauge data will be inaccurate.</p>
<p>Three 10uF filter capacitors should be connected in parallel to VPH_PWR close to the PM7250B charging chip.</p>
<p>Connect the 1K resistor in series between the USB_DP/DM of the PM7250B charging chip and the USB_DP/DM of the module. Pay attention to the position of the 1K resistor when laying out to prevent the traces of USB_DP/DM from bifurcating.</p>
<p>CC1 and CC2 are connected to the CC pin of the Type-C connector, and a 220pF filter capacitor needs to be connected in parallel.</p>
<p>TYPEC_VBUS_IN should be pulled down to GND through a 56K resistor to quickly discharge when the charging cable is disconnected, and a 1uF filter capacitor should be connected in parallel.</p>
<p>The maximum working voltage of the TVS and capacitor connected in parallel with TYPEC_VBUS_IN should match its input voltage range. For example, if the maximum input voltage is 12V, a TVS with a working voltage of 15V and a capacitor with a working voltage of 25V should be selected.</p>

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<input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>	Only modules using X62 and X65 platforms support the EBI interface, but the software of standard version modules does not support this function. The EBI2 interface is shared with the internal NAND of the module, please do not pull up or pull down any signal of this interface.
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<input type="checkbox"/> YES	<input type="checkbox"/> NO	<input type="checkbox"/> NA	<p>All modules support dual USIM interfaces, but only the SIM8200G module reserves the eSIM chip connected to the internal USIM2 interface.</p> <p>Please refer to the Hardware Design Guide for more information.</p>
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No	Check Items
1	General inspection
2	VBAT_BB VBAT_RF
	VDD_EXT
3	PWRKEY circuit
4	RESET circuit

5	USB signal circuit
6	PCIE signal
7	WIFI
8	Audio circuit

9	SPI
10	I2C
11	RGMII
12	EBI2
13	ADC
14	NTC
15	SD/SDIO
16	USIM
17	GPIO signal

18	GND
19	RF circuit

20	Charging circuit
21	Differential Signal
22	Other

315/X55/X65/X62 Series 5G LGA Module PCB Layout Check List

Detailed check contents
Confirm whether the module PCB package provided by SIMCom are used. If the customer designs the package by himself, make sure that the package is correct.
Avoid 90-degree routing, use 135-degree or smooth arc routing to reduce signal reflection.
For RF, USB, PCIE, RGMI and other signal impedance control, PCB is recommended to use at least 6-layer HDI stack-up structure.
Must check whether the customer's heat dissipation design measures meet the requirements of 5G modules. For example: 1.The LGA module should be kept away from the heat source. 2.Not to place components on the back of the PCB board with the LGA module. Reserve enough copper on the BOTTOM side of the Main PCB for adding thermal silical to better transmit heat to Heat Sink or Metal housing. For detailed design of heat dissipation, please refer to <SIMCom_Module_Thermal_Design_Guide>
The filter capacitors of VBAT_BB and VBAT_RF should be placed close to their respective pins, the smaller the closer to the pins, the power supply trace should first pass through the large capacitor, then pass through the small capacitor, and finally reach the VBAT_BB or VBAT_RF pin of the module.
The VBAT power supply requires star route, which needs to be led out from the battery connector or the output capacitor end of the LDO/DC-DC power supply. (For example, 5G module and QTM545/547 and W82 etc,VBAT need star route)
VBAT_BB is the baseband power input of the module, and the trace width must be greater than 2mm. DC ESR as low as possible. VBAT_RF is the RF power input of the module, and the trace width must be greater than 3mm. DC ESR should be as low as possible.
The VBAT parallel TVS should be placed close to the module pins, and the GND pin of the TVS must be directly connected to the GND main plane. The VBAT trace must pass through the pin of TVS first and then connect to the VBAT pin of the module.
VBAT traces should be kept away from sensitive signals, especially RF, Audio, USB, PCIE, CLK, SDIO, RGMII, SPMI, EBI, etc.
Note that the width of the GND trace on the VBAT main return path must also ensure sufficient overcurrent capability. It is recommended to use the GND plane and add enough vias when changing layers.
The VDD_EXT trace should be connected to the module pin in series with a resistor and then connected to TVS in parallel before supplying power to the peripheral components.
In order to prevent the DC voltage drop from being too large, it is recommended that the trace width be greater than 0.25mm.
Pay attention to protecting the PWRKEY traces, and the following measures can be taken: be isolated with ground, avoid being parallel to other signal traces, keep away from the edge of the board, and avoid excessively long surface traces.
The PWRKEY trace should pass through the TVS before connecting to the module PWRKEY pin. If a key is used, the TVS is placed close to the key.
Pay attention to protecting the RESET traces, and the following measures can be taken: be isolated with ground, avoid being parallel to other signal traces, keep away from the edge of the board, and avoid excessively long surface traces.
The RESET trace should pass through the TVS before connecting to the module RESET pin. If a key is used, the TVS is placed close to the key.
EMI suppression components (such as TVS, common mode inductor) should be placed close to the USB connector, and the traces should first pass through the TVS and then connect to the relevant USB pins of the module.

The edge rate of the USB signal is very fast, so keep away from sensitive signals such as RF, audio, and clock.
The USB connector should be far away from the RF antenna, especially the 2.4G antenna, and the two should be well isolated.
The USB_HS_DP/M traces must control 90 ohm differential impedance, and the difference between the lengths of the two traces in the differential pair should be less than 0.7mm. The trace length is less than 100mm, and the number of vias is less than 2. Avoid forked traces affecting USB speed and recognition.
The USB_SS_RX_P/M, USB_SS_TX_P/M traces must control 85 ohm differential impedance, and the difference between the lengths of the two traces in the differential pair should be less than 0.7mm. The trace length is less than 100mm, and the number of vias is less than 2. Avoid forked traces affecting USB speed and ..
The AC capacitor in series with USB_SS should be placed close to the output pin for signal integrity. The two AC capacitors connected in series on each differential pair should be parallel and placed symmetrically close together, otherwise it may affect signal integrity and cause EMI problems.
The trace distance between RX and TX of USB_SS, between USB_SS/HS and other signals should not be less than 4 times the trace width.
Differential signals should be routed on the inner layer as much as possible, be isolated with stiched ground on both sides and solid ground on the adjacent PCB layers from end-to-end.
The USB connector should be close to the module and the traces should be as short as possible.
All high-speed or sensitive signals should be kept away from PCIE traces to prevent interference by them.
The PCIE_RX0_P/M、PCIE_RX1_P/M、PCIE_TX0_P/M、PCIE_TX1_P/M、PCIE_REFCLK_P/M traces must control 85 ohm differential impedance, and the difference between the lengths of the two traces in the differential pair should be less than 0.5mm. The trace length is less than 150mm.
When the PCIE_RX0_P/M and PCIE_RX1_P/M signals are used at the same time, should control equal length; When the PCIE_TX0_P/M and PCIE_TX1_P/M signals are used at the same time, should control equal length. There is no need to control equal length between PCIE_TX, PCIE_RX and PCIE_REFCLK.
The AC capacitor in series with PCIE should be placed close to the output pin for signal integrity. The two AC capacitors connected in series on each differential pair should be parallel and placed symmetrically close together, otherwise it may affect signal integrity and cause EMI problems.
The trace distance between each differential pair of PCIE and between other signal traces should not be less than 4 times the trace width.
Differential signals should be routed on the inner layer as much as possible, be isolated with stiched ground on both sides and solid ground on the adjacent PCB layers from end-to-end.
Under the premise of meeting the thermal design requirements, the WIFI module should be properly close to the 5G module, shorten the power trace of the WIFI module, and reduce the DC ESR and voltage drop of the power trace.
The VBAT trace width of the WIFI module should be greater than 1.5mm.
The capacitor (10uF+1uF+100nF) connected in parallel to WL_VDD_VM should be placed close to the WIFI module, and the trace width should be greater than 0.6mm.
The capacitor (10uF+1uF+100nF) connected in parallel to WL_VDD_VL should be placed close to the WIFI module, and the trace width should be greater than 2mm. The DC ESR of the trace should be less than 5mΩ.
The capacitor (10uF+1uF+100nF) connected in parallel to WL_VDD_VH should be placed close to the WIFI module, and the trace width should be greater than 0.6mm.
SLEEP_CLK is the sleep clock of the module. The trace should be routed on the inner layer as much as possible, be isolated with stiched ground on both sides. Keep away from sources of interference such as power supplies, RF and high-speed signals.
I2S/PCM signals should be routed in a group and on the inner layer as much as possible, be isolated with stiched ground on both sides. Keep away from sources of interference such as power supplies, RF and high-speed signals.
The I2S_MCLK trace should be routed on the inner layer as much as possible, be isolated with stiched ground on both sides. Keep away from sources of interference such as power supplies, RF and high-speed signals.

SPI signals should be routed in a group and be isolated with stiched ground on both sides as possible. Keep away from sources of interference such as power supplies, RF and high-speed signals.
The SPI_CLK trace should be routed on the inner layer as much as possible, be isolated with stiched ground on both sides. Keep away from sources of interference such as power supplies, RF and high-speed signals.
I2C signals should be isolated with stiched ground on both sides as much as possible. Keep away from sources of interference such as power supplies, RF and high-speed signals.
The RGMII_RX and RGMII_TX traces should control 50 ohm single-ended impedance. The length difference between TX_CLK and TX_CTL/TX_DATA traces should be less than 5mm. The length difference between RX_CLK and RX_CTL/RX_DATA traces should be less than 5mm. All trace length should be less than 100mm.
The trace distance between all RGMII signals should be no less than 2 times the trace width. The trace distance between all RGMII signals and other signals should be no less than 3 times the trace width.
RGMII_RX and RGMII_TX should be routed in a group respectively and on the inner layer as much as possible, be isolated with stiched ground on both sides. RX_CLK and TX_CLK should be routed on the inner layer and be isolated with stiched ground on both sides individually.
The EBI2_AD[0:7], EBI2_WE_N, EBI2_CLE, EBI2_RE_N, EBI2_CS traces should control 50 ohm single-ended impedance. The length difference between each signal should be less than 5mm. All trace length should be less than 80mm.
ADC signals should be routed on the inner layer and be isolated with stiched ground on both sides. Keep away from sources of interference such as power supplies, RF and high-speed signals.
The NTC resistor should be placed close to the object or area that needs temperature measurement. The NTC temperature detection signal is an analog signal, which should be routed on the inner layer and be isolated with stiched ground on both sides. Keep away from sources of interference such as power supplies, RF and high-speed signals. The NTC resistor avoid sharing the return path with the large current on the GND plane, and it should be directly connected to the ground of the module as much as possible.
The distance between each signal of SD/SDIO should not be less than 2 times the trace width. Keep away from sources of interference such as power supplies, RF and high-speed signals.
The trace width of the SD card power supply should meet the current requirements. If it needs to support SD3.0, it is recommended that the trace width be greater than 0.8mm. (Please increase the trace width appropriately according to the working current of the SD card used)
The SD/SDIO traces should control 45 ohm single-ended impedance.
The length difference between CLK and DATA/CMD should be less than 1mm. If the CLK frequency is 208MHz, the trace length of all SD/SDIO signals should be less than 40mm.
All traces of SD/SDIO should pass through TVS first and then connect to the module.
CLK signals should be routed on the inner layer and be isolated with stiched ground on both sides. Keep away from sources of interference such as power supplies, RF and high-speed signals.
All signals of USIM card interface should be routed on the inner layer and be isolated with stiched ground on both sides as much as possible. Avoid parallel routing with high current traces and high frequency signals.
The SIM_CLK signal of USIM card interface should be routed on the inner layer individually and be isolated with stiched ground on both sides as much as possible. Keep away from the edge of the board and other high current traces and high frequency signals, do not run parallel routing under the shield to avoid ESD and other
The TVS should be placed close to the USIM card socket, and the traces pass through the TVS first and then connect to the module.
The power and signal of the USIM avoid sharing the return path with the large current on the GND plane.
Note that the area under the shrapnel of the USIM card socket should be cleared to prevent long-term wear and tear from causing a short circuit with the motherboard.
If GPIO is configured as an interface such as SPI, UART, I2C, I2S, etc., the traces should be routed in groups according to the interface to which the signal belongs. Each group of signals should be isolated with stiched ground on both sides, and the high-speed clock should be isolated separately.

The ground plane near and below the module should be complete, and the number of ground vias should be sufficient, especially under the high-power chip of the module.
The GND pad and the GND plane can be connected by thermal pad, but the connection must be sufficient.
The TVS should be connected to the main ground plane of the PCB as close as possible to reduce the grounding impedance as much as possible.
Make sure the main GND plane is not damaged and the connectivity is good.
Make sure there are enough ground vias on the path from the main GND layer to the main GND of the module.
The GND pad in the middle of the module should be designed with enough GND vias to facilitate the heat dissipation of the module.
GND (Pin AH45, AG47, AF45, AE47, AD49, AB49.AA51, W51, U51, T49, R47) is the ground return pin of VBAT. These pins should be placed with a large enough ground plane and enough vias to Ensure a low impedance return path.
ANT traces should control 50 ohm single-ended impedance.
Under the premise of ensuring the impedance requirement, the ANT trace should be as short and wide as possible, which can reduce the PCB insertion loss in the high frequency band.
ANT traces and antenna areas should be kept away from power, clock, audio and other interference sources and sensitive signals, and ensure sufficient isolation.
The distance between the ANT trace and GND should be kept at 2 times trace width, and the distance between the ANT trace and other signal traces should be kept at least 5 times trace width. Place GND vias on the ground traces or ground plane around the ANT trace at intervals of 1/10 the signal wavelength.
It is best not to change layers for ANT traces, because each hole will cause at least 15% signal reflection, resulting in impedance discontinuity.
It is best not to place any vias in the vertical projection area of the ANT trace on the reference ground plane, otherwise it will deteriorate the flatness of the reference ground plane and affect the impedance. If the ANT trace refers to the surface ground plane, and there is a GND pad of the device directly above, the solder paste after the component is soldered will affect the continuity of the ANT impedance.
The copper layer at least 450um below the ANT pin must be cleared to reduce the influence of the parasitic capacitance formed by the ANT pad and the reference ground plane on high-frequency signals
If ANT_CTRL0, ANT_CTRL1, RFFE0_DATA, and RFFE0_CLK are configured as RFFE3_CLK/RFFE3_DATA to control the antenna tuner, the traces should control the 50-ohm single-ended impedance and be isolated with stitched ground on both sides, away from power, high-speed, switch, audio and other signals. The distance between RFFE_DATA and RFFE_CLK traces should be at least 2.5 times trace width, and the length difference should not exceed 1mm. The distance between RFFE and other signal traces should be at least 2.5 times trace width. The capacitance of the RFFE_MIPI trace should be less than 50pF.
mmW intermediate frequency signal IFV and IFH traces must control 50 ohm single-ended impedance, and ensure the isolation of IF signal in design.
The IFV and IFH traces of the same QTM antenna module must control the length difference within 0.2mm.
In order to reduce PCB trace loss, under the premise of ensuring the impedance requirement, the trace width of IFH and IFV should be kept at least 10mil.
In order to ensure low trace loss of IFH and IFV (QTM545<6dB, QTM547<1.5dB), it is recommended to use low-loss coaxial cables or mmW special PCB boards.
The QTM antenna module has a large thermal power, so heat dissipation measures should be taken into consideration during design.
When designing, the isolation between QTM and GNSS, LTE, Sub-6 and other antennas should be considered, and the coexistence design should be considered.
The PM7250B charging chip should be placed close to the battery connector to avoid that the VBAT route too long, which may lead to inaccurate charging voltage and current detection

SPMI_CLK and SPMI_DATA must control the 50-ohm single-ended impedance and be isolated with stitched ground on both sides. The distance between SPMI_CLK and SPMI_DATA or between SPMI and other signals should be 2 times trace width. The length difference between SPMI_CLK and SPMI_DATA should be less than 1mm, and the traces length should not exceed 70mm.

VBATT_SNS_P/M should be connected directly to the battery connector. VBATT_SNS_P/M signal should be routed on the inner layer and be isolated with stitched ground on both sides.

BATT_ID signal should be isolated with stitched ground on both sides. Keep away from sources of interference such as power supplies, RF and high-speed signals.

BATT_THERM signal should be isolated with stitched ground on both sides. Keep away from sources of interference such as power supplies, RF and high-speed signals. The NTC resistor should take shielding measures and be as close to the battery as possible, away from the heat source of the battery protection board to ensure the temperature detection accuracy.

The NTC resistor avoid sharing the return path with the battery power supply, and should be connected directly to the module with a separate trace, and the battery uses a separate pin to connect to the NTC GND. (Pay attention to check the GND trace of the NTC resistor on the battery protection board)

AMUX_1 signal should be isolated with stitched ground on both sides. Keep away from sources of interference such as power supplies, RF and high-speed signals. The NTC resistor is placed close to the PM7250B charging chip.

CONN_THERM signal should be isolated with stitched ground on both sides. Keep away from sources of interference such as power supplies, RF and high-speed signals. The NTC resistor is placed close to the Type-C connector, paying attention to keep it away from heat sources.

The trace width of VPH_PWR supplying power to the module should be greater than 4mm.

The USB_DP/DM trace between the PM7250B charging chip and the module should avoid bifurcating at the 1K resistor in series.

When the maximum charging current is required, the width of the TYPEC_VBUS_IN trace should be greater than 4mm.

All TVS should be placed close to the connector, and the traces should pass through the TVS before connecting to the module. The TVS should be connected to the main ground plane as close as possible to reduce the grounding impedance.

Differential pairs should be routed in parallel as much as possible to ensure that the two traces are tightly coupled.

If the differential pair needs to control the equal length through serpentine routing, please route the serpentine wire at the fan-out end of the module or the connector end, do not wrap the serpentine wire in the middle of the routing, and try to ensure the equal length and equidistance requirements of the differential signals.

The test points, capacitors, resistors, TVS, and other components connected by the differential pair should be parallel and placed symmetrically close together to prevent impedance mismatch and EMI problems.

When the differential pair is connected to components such as test points, capacitors, resistors, TVS, and common mode inductors, avoid trace forks.

The differential pair should minimize the number of punching and layer changes, and the vias should be placed symmetrically.

Customers need to control the PCB warpage to no more than 0.3% during the design and processing stages to avoid poor module soldering.

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No	Check Items	
1	General inspection	
2	Power supply	VBAT (Pin2/4/70/72/74)
		VIO_1V8 (Pin 65)
3	Start-up circuit	FULL_CARD_ POWER_OFF# (Pin 6)
4	RESIN N circuit	RESET# ---

		(Pin 67)
5	USB interface	USB3.0/1 (Pin29/31/35/37)
		USB2.0 (Pin7/9)
		TYPEC positive and negative identification function
		USB_VBUS
	PCIE interface	PCIE (Pin41/43/47/49/53/55)
		PEWAKE# (Pin54)
		PERST# (Pin50)
		CLKREQ# (Pin52)

6		Level shift
	PCIE module and AP indication status signal	SDX2AP_STATUS (Pin T7)
		AP2SDX_STATUS (Pin V7)
		SDX2AP_EP11_STATUS (Pin AG5)
		SDX2AP_ERR_FATAL (Pin U5)
		AP2SDX2_ERR_FATAL (Pin R5)
		WAKE_UP_IN (Pin AE5)

7	W82/W80 interface	Coexistence signal (When the 5G module and the WIFI module share the antenna and the isolation is not higher than 15dB, the coexistence signal needs to be used; when the 5G module and the WIFI module do not share the antenna and the isolation is higher than 15dB, the coexistence signal does not need to be used)
		WL_VDD_VM (Pin Z16/17/18)
		WL_VDD_VL (Pin Z20/21/22/23/24/25)
		WL_VDD_VH (Pin Z27/28/29)
		Other signal
8	UART interface	UART1_RX(Pin62) UART1_TX(Pin64)
		I2C_SDA(Pin68)

9	I2C circuit	I2C_SDA(Pin100) I2C_SCL(Pin38)
10	Audio interface	I2S/PCM
11	SPI interface	SPI
12	USIM card interface	(U)SIM1_VDD(Pin 36) (U)SIM2_VDD(Pin 48)

		(U)SIM
13	DRP	DRP (Pin 25)
14	WoWWAN#	WoWWAN# (Pin 23)
15	LED1#	LED1# (Pin 10)
16	W_DISABLE1#	W_DISABLE1# (Pin 8)
17	W_DISABLE2#	W_DISABLE2# (Pin 26)
18	TDD_SYNC_PPS	TDD_SYNC_PPS (Pin 26)
19	PCIE_DISABLE	PCIE_BOOT_DISABLE (Pin38)
20	Lenovo customized version special definition PIN	VIO_1P8 (Pin24)
21		DRP2 (Pin28)
22		ANTCTL4 (Pin22)
23	CONFIG	CONFIG
24	GPIO	GPIO

25	RF circuit	RF circuit
		mmW circuit

315/X55/X65/X62 Series 5G M.2 Module Schematic Check List

Detailed check contents
Confirm whether the schematic symbols of M.2 connector provided by SIMCom are used. If the customer designs the symbol by himself, make sure that the symbol is correct.
If the function of the GPIOs used by the customer is inconsistent with the default of SIMCom, the application information of these GPIOs should be provided to SIMCom for inspection.
Module main power input. The voltage range is 3.135V~4.4V, the typical voltage is 3.8V, and the continuous supply current is at least 3A.
It is recommended that the module use a dedicated DC/DC switching regulators, which is not shared with other loads. If the VBAT network is connected to other DC/DC switching regulators inputs, it is recommended to use magnetic beads to separate the VBAT network from other DC/DC switching regulators input to reduce
The total capacitance value of the capacitor placed near the VBAT pin of the module shall be greater than 420uF to ensure that when the module VBAT is at 3.8V and the maximum power consumption, the input voltage is not lower than 3.135V after an instantaneous (ms level) drop. If the customer uses 3.3V or USB2.0 (5V/500mA) interface for power supply, in order to ensure the normal operation of the module, it is recommended to increase the VBAT capacitor to more than 1mF.
In addition to parallel high value capacitors, incorporate a group of small capacitors to filter out high-frequency interference, and at least reserve space for components during design. (1uF+100nF+100pF+33pF combination is recommended)
In order to improve the ESD and surge protection capability of the module, it is recommended to use a TVS whose Vrwm is 4.8V or 5V. The clamping voltage should be as close as possible to the input voltage of the module, while ensuring that Ipp is high enough. For example, TVS WS4.5DPV, when VC=7V, IPP=80A.
If the motherboard uses a DC adapter to cooperate with the power conversion circuit to supply power to the module, TVS must be used at the interface of the DC adapter, and Vrwm is not lower than the maximum output voltage of the DC adapter.
1.8V power output. It is mainly used as the power supply for pulling up the module pin, and the maximum output current is 50mA.
The total capacitance in parallel with this pin should be less than 2.2uF.
It is recommended to connect a 0R resistor in series close to VIO_1V8, then connect TVS (Vrwm: 2.5~3V) in parallel and then connect the load. To further improve the ESD protection capability of this pin, replace the 0R resistor with 2.2R. This pin is very sensitive to static electricity and surge, please pay attention to protection. When VIO_1V8 is used to supply power to the VDD_IO of the W82/W80 WIFI module, the resistance in series in the middle must be 0R to prevent the resistance from dividing the voltage, resulting in IO levels that do not meet the requirements of electrical characteristics.
When FULL_CARD_POWER_OFF# keeps high level, the module turns on; when it keeps low level, the module turns off. The high level of this pin is 1.8~4.4V, pay attention to level matching when designing. Note: For modules using the X55/315 platform and the SIM8260A-M2 module, if you connect FULL_CARD_POWER_OFF to VBAT to power on and start up, you need to connect a 1K resistor in series in the middle. When the module crashes and the software is forced to be downloaded, the 1K resistor needs to be disconnected after VBAT is powered on for 2 seconds to ensure that the port changes to 9008 and force the software to be upgraded.
The GPIO of the AP can be used to turn on or off the module. (as shown in the right figure)
You can use a self-locking button or a toggle switch to turn on or off the module. The button needs to be connected to a TVS in parallel. The junction capacitance of the TVS is recommended to be less than 10pF.
Module reset signal input, active low. This pin is pulled up to VIO_1V8 through a 10K resistor inside the module, pay attention to level matching when designing. (SIM8260C-M2 module has no internal pull-up, and must be pulled up to VIO_1V8 by adding a 10K resistor externally)

The GPIO of the AP can be used to reset the module.
Buttons can be used to reset the module, and the buttons need to be connected to TVS in parallel.
The USB_SS_RX_P/M and USB_SS_TX_P/M differential pairs must adopt 85 ohm differential impedance control, and the difference between the lengths of the two traces of the differential pair should be less than 0.5mm. These requirements should be marked on the schematic diagram. If USB_SS is connected to a USB connector (such as Type-C, etc.), TVS must be connected in parallel close to the connector to provide ESD protection, and the TVS junction capacitance must be less than 0.5pF.
The USB_SS signal requires an AC capacitor connected in series between the transmitter and receiver for AC coupling, and the capacitor should be as close to the transmitter as possible. USB_SS_TX_P/M has a pair of 220nF AC capacitors connected in series inside the module, no external capacitors are needed; If the USB_SS_RX_P/M is directly connected to the IPQ or AP chip, a 220nF AC capacitor needs to be connected in series near the IPQ or AP end.
Notice: When connected to the USB female connector, connect USB_SS_TX to TX, and USB_SS_RX to RX (because the Type-C/A cable internally crosses TX and RX). When connecting a USB male connector and a chip such as IPQ or AP, USB_SS_TX is connected to RX, and USB_SS_RX is connected to TX. Please confirm the differential pair between the module and the peer device (module, chip, connector, etc.), P is connected to P, and N is connected to N.
The USB_HS_DP/M differential pair must adopt 90 ohm differential impedance control, and the difference between the lengths of the two traces of the differential pair should be less than 0.7mm. These requirements should be marked on the schematic diagram. If USB_HS is connected to a USB connector (such as Type-C, etc.), it is recommended to connect TVS in parallel close to the connector, and then connect it to the module in series with a common mode inductor (DLW21SN670SQ2L, MURATA) to provide ESD protection and suppress common mode noise. The TVS junction capacitance must be less than 0.5pF. If the USB_HS_DP/M is connected to the AP chip, it is recommended to connect a 0 ohm resistor in series for easy commissioning. Please confirm the differential pair between the module and the peer device (module, chip, connector, etc.), P is connected to P, and N is connected to N. (The USB2.0 interface must be drawn out for forced firmware update)
When the module USB_SS is connected to the Type-C connector: PEWAKE# (Pin 54) can be reused to receive the ID signal of the CC chip. CLKREQ# (Pin 52) can be reused to receive the interrupt signal of the CC chip. PERST# (Pin 50) can be reused to send the switching signal of the USB_SS switch. (Note: The level of the standard version module is 3.3V and does not support this function by default. To enable this function, a special customized version is required)
Note: The interface of the M2 module using the X62/X65/X55/315 platform does not have a USB_VBUS pin.
Support 1 lane PCIe3.0, 8Gbps per lane, backward compatible with PCIe2.0 and PCIe1.0.
PETp/n0、PERp/n0、REFCLKP/N differential pairs must adopt 85 ohm differential impedance control, and the difference between the lengths of the two traces in the differential pair should be less than 0.5mm. These requirements should be specified Identified in the schematic.
The PCIe signal needs to be AC-coupled by connecting an AC capacitor in series between the transmitter and the receiver, and the capacitor should be as close as possible to the transmitter. PETp/n0 have connected 220nF AC capacitor in series inside the module, no external capacitor is needed. PERp/n0 must be connected in series with a 220nF AC capacitor at the opposite chip pin of the module.
This pin is signal input when the module is in RC mode. This pin is a signal output when the module is in EP mode. 3.3V level, pay attention to level matching when designing, and must be pulled up to 3.3V through a 10K resistor.
This pin is signal output when the module is in RC mode. This pin is a signal input when the module is in EP mode. 3.3V level, pay attention to level matching when designing.
This pin is signal input when the module is in RC mode. This pin is a signal output when the module is in EP mode. 3.3V level, pay attention to level matching when designing, and must be pulled up to 3.3V through a 10K resistor.

The module integrates a 1.8V to 3.3V level conversion circuit inside, but there is no 3.3V power supply, so an LDO is needed to provide a 3.3V power supply for the level conversion chip.

Note: When the following conditions exist at the same time, the computer cannot be shut down.

1. The enable pin of the LDO is controlled by VIO_1V8 and the LDO has an output discharge function. When the computer is turned off, VIO_1V8 stops outputting, the output of LDO is short-circuited to GND, and the PCIE_WAKE signal is forcibly pulled down by the output of LDO.

2. When PCIE_WAKE is at low level, the computer system mistakenly believes that the module is still transmitting data, and will restart the computer.

If NMOS is used to implement level conversion, the level of G should be consistent with that of S.(as shown in the right figure)

Signal output. When the module is turned on normally and successfully registered with the network, this pin outputs a high level to the AP. When the module is turned on or registered with the network abnormally, this pin outputs a low level to the AP.

Signal input. When the AP is turned on normally, this pin outputs a high level to the module. When the AP is turned on abnormally, this pin outputs a low level to the module.

Signal output. When the module can make an emergency call, this pin outputs a high level to the AP.

Signal output. When the module has a fatal error, this pin outputs high level to the AP.

Signal input. When the AP has a fatal error, this pin outputs high level to the module.

signal input. When the module sleeps, pull this pin low to wake up the module.

WAKE_UP_IN, TDD_SYNS and W_DISABLE2 share PIN26, and only one of them can be supported at the same time. (The software of the standard version module supports TDD_SYNS by default)

The COEX_UART_TXD(Pin 64),COEX_UART_RXD(Pin 62) serial port signals are the coexistence signals of the LTE frequency band of the module and the 2.4G frequency band of the WIFI module. Pay attention to the signal direction when designing.

This signal shares Pin 64 and Pin 62 with UART1, and they can only support one of them. (The hardware of the standard version module supports UART1 by default)

The output signal of LAA/N79_TX_EN and the input signal of WL_TX_EN are the coexistence signals of the LAA/N79 frequency band of the module and the 5G frequency band of the WIFI module. Pay attention to the signal direction when designing.

The software of the standard version module does not configure coexistence signals by default.

Power Output. The maximum output current is 0.6A, only for SIMCom W82/W80 WIFI module.

WL_VDD_VM should be connected in parallel with 10uF+1uF+100nF capacitor.

Power Output. The maximum output current is 1.7A, only for SIMCom W82/W80 WIFI module.

WL_VDD_VL should be connected in parallel with 10uF+1uF+100nF capacitor.

Power Output. The maximum output current is 0.6A, only for SIMCom W82/W80 WIFI module and mmW QTM antenna module.

WL_VDD_VH should be connected in parallel with 10uF+1uF+100nF capacitor.(When used for WIFI module)

For other control signal design principles, please refer to the hardware design guidelines and reference designs.

UART1_RX (Pin62) and UART1_TX (Pin64) are 2-wire serial ports, and it is necessary to confirm whether the interface definition of the peripheral and the signal direction are consistent;

The software default UART is closed, and it can be enabled by AT+ccuart=1 command.

UART working level is 1.8V, please pay attention to level matching when designing.

When the baud rate of the UART interface is more than 460Kbps, it is not recommended to use transistors for level conversion

The UART interface rate is up to 4Mbps, and cannot be used for higher rate requirements, 115200bps is recommended.

I2C working level is 1.8V, please pay attention to level matching when designing.

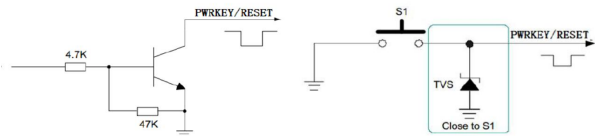
If it is connected to a level conversion chip, make sure that the chip meets the I2C transmission rate requirements.

If you are not sure whether the pull-up resistor is integrated inside the level conversion chip used, it is

<p>Confirm whether the pull-up resistor value meets the requirements of the communication rate, and the module pulls up to VIO_1V8 through a 2.2K resistor inside the module. (SIM8260C-M2 module does not have an integrated pull-up resistor, it must be pulled up to VIO_1V8 through a 2.2K resistor externally)</p>
<p>The device address on the same group of I2C cannot be the same .</p>
<p>Verify that the I2S/PCM signal and the peripheral are connected correctly, pay special attention to the direction of the signal. (Default only supports I2S)</p>
<p>By default, the module supports two I2S interfaces with 48KHz sampling rate and 16-bit sampling depth.</p>
<p>The pin definition of I2S/PCM interface is as follows. Pin20:I2S_SCLK/PCM_CLK Pin22:2S_RX/PCM_DIN Pin24:I2S_TX/PCM_DOUT Pin26:I2S_WA/PCM_SYNC Pin60:I2S_MCLK</p>
<p>If the audio CODEC chip used is not recommended by SIMCom, please contact SIMCom for evaluation.</p>
<p>Verify that the SPI signal and the peripheral are connected correctly, pay special attention to the direction of the signal.</p>
<p>The SPI interface of the module only supports master mode, and the rate is up to 50MHz.</p>
<p>The following pins can be customized as SPI interface, and the VOIP function can be extended by connecting the LE9643 chip. Pin25:SPI_MISO Pin38:SPI_CLK Pin60:SPI_MOSI Pin25:SPI_CS_N (The hardware of the standard version module does not support SPI by default, and a special customized version is required to enable the SPI interface)</p>
<p>1.8/3.0V dual voltage self-adaptive output, suitable for (U)SIM cards with different voltages.</p>
<p>Pay attention to the load capacitors of (U)SIM1_VDD and (U)SIM2_VDD have a capacitance range of 100nF-470nF and should be placed close to the (U)SIM card socket (220nF+33pF is recommended).</p>
<p>Confirm the load capacitance of the (U)SIM signal (parallel capacitance, TVS parasitic capacitance, series resistance, etc.), and test the rising edge Tr and falling edge Tf of (U)SIM_CLK. (U)SIM_CLK: Tr<50ns Tf<50ns. The initial voltage of (U)SIM_VDD is 1.8V. When the (U)SIM card is detected, if the waveform of (U)SIM_CLK is bad, the (U)SIM card may not be recognized. The voltage of (U)SIM_VDD will increase to 3V and the card will be recognized again. If the (U)SIM card inserted at this time is 1.8V, the (U)SIM card may be damaged.</p>
<p>(U) SIM1_CLK (Pin 32), (U) SIM1_DATA (Pin 34), (U) SIM1_RESET (Pin 30) are connected in series with 22R resistors and reserve 15pF filter capacitors. It is generally recommended that filter capacitors not be assembled, and ensure that the total capacitance (parasitic capacitance and filter capacitor) of CLK and DATA signals is not greater than 30pF.</p>
<p>(U) SIM1_CLK (Pin 44), (U) SIM1_DATA (Pin 42), (U) SIM1_RESET (Pin 46) are connected in series with 22R resistors and reserve 15pF filter capacitors. It is generally recommended that filter capacitors not be assembled, and ensure that the total capacitance (parasitic capacitance and filter capacitor) of CLK and DATA signals is not greater than 30pF.</p>
<p>(U)SIM_DATA has been pulled up to (U)SIM_VDD through a 20K ohm resistor inside the module. The peripheral circuit of the module should reserve the 10K pull-up resistor that is not assembled.</p>

<p>(U)SIM1_DET(Pin 66), (U)SIM2_DET(Pin 40) are used for (U)SIM card hot plug detection. To use the hot-swap function, these two pins should be pulled up to VDD_VIO through a 100K resistor.</p> <p>The software default configuration, when the (U)SIM card is not inserted, (U)SIM_DET and GND are short-circuited, after the (U)SIM card is inserted, (U)SIM_DET and GND are open, and (U)SIM_DET changes from low level to high level, that is, the rising edge Valid (you can use the AT+UIMHOTSWAPLEVEL=0 or 1 command to change this logic to adapt to different (U)SIM card sockets).</p> <p>The hot swap function is disabled by default in the software (you can use the AT+UIMHOTSWAPON=1,1 command to enable the card slot 1 hot swap function; you can use the AT+UIMHOTSWAPON=1,2 command to enable the card slot 2 hot swap function).</p>
<p>All pins of the (U)SIM card socket need to add TVS to ensure ESD protection capability (the junction capacitance of the ESD protection component should be less than 15pF).</p>
<p>Check the connection relationship between the module and the (U)SIM card socket, and whether the package of the (U)SIM card socket is correct.</p>
<p>Signal input. It is used to receive the SAR sensor interrupt signal, so that the module can adjust the output power.</p> <p>SAR Specific Absorption Rate is a radiation indicator. When the module is close to the head or body, the capacitance sensed by the SAR sensor increases, and an interrupt signal will be sent to the 5G module through the DRP, and the 5G module will reduce the transmission power until the SAR index meets the requirements to <u>protect the human body from excessive radiation</u>.</p>
<p>Open-drain output. It needs to be pulled up to the HOST voltage through a 10K~100K resistor outside the module. When the module receives phone calls, text messages and other information, pull it low for 1s to wake up HOST.</p>
<p>Open-drain output. Indicate the network status of the module through the external LED. The maximum drive current is 3mA, if you need a higher drive current, please use it in series with PNP transistors or PMOS.</p>
<p>Signal input. When the input is low, the module enters flight mode.</p>
<p>Signal input. When the input is low, the module turns off GNSS (the old version SIM8200EA-M2-ANT4/6 and SIM8300G-M2-5/-7 only support W_DISABLE2#, which can be driven by 1.8V or 3.3V GPIO, and the low level is active) .</p> <p>If the module using the X65/X62 platform needs to support W_DISABLE2#, since its level is 1.8V, when the connected GPIO is 3.3V, a diode needs to be connected in series, and the N pole is connected to the 5G module.</p> <p>(The hardware of the standard version module does not support this function, and this pin is used for TDD_DYNAMIC_BAND_SELECTION)</p>
<p>Signal output. Output a pulse every second to indicate the uplink and downlink frame flag of the 5G TDD band.</p>
<p>The default drive current is 2mA</p>
<p>Signal input. When the input is high, it enters the PCIE identification mode.</p> <p>(The hardware of the standard version module does not support this function, and this pin is used for I2C_SCL by default)</p>
<p>Lenovo customized version, power output, used for 1.8V power supply for antenna tuner.</p>
<p>Lenovo customized version, signal input, used to receive the interrupt signal of the second SAR sensor.</p>
<p>Lenovo customized version, signal output, used to control the antenna tuner.</p>
<p>CONFIG_0 (Pin 21), CONFIG_1 (Pin 69), CONFIG_2 (Pin 75) are connected to GND inside the module, and CONFIG_3 (Pin 1) is not connected inside the module, that is, the configuration of the M.2 interface of the module is WWAN-USB3.0/PCIE Types.</p>
<p>Interfaces such as I2S/I2C/UART can be configured as GPIO. For more information, please refer to the hardware design guide. If the usage requirements are different from the functions supported by the pin by default, please provide the usage requirements to SIMCOM to confirm whether it can be configured.</p> <p>(Note that the I2C interface is pulled up inside the module, you should confirm whether it affects its secondary development for GPIO)</p>

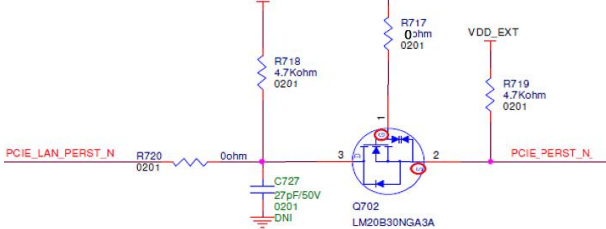
The RF circuit requires a π -type matching circuit. The module has a variety of antenna quantity specifications such as 4 antennas, 5 antennas, or 6 antennas. For more information, please refer to the hardware design guide.
The correctness of the antenna matching circuit, tuner circuit, and SAR sensor circuit needs to be confirmed with the RF engineer.
The RF frequency band, CA combination, and antenna frequency band allocation supported by the module need to be confirmed with the RF engineer.
ANT_CTRL0, ANT_CTRL1, RFFE0_DATA, and RFFE0_CLK are used by default for the antenna tuner, and it is not recommended to use them for other purposes.
If ESD protection design is considered, TVS can be used, and the TVS junction capacitance should be less than 0.05pF. (To avoid affecting RF performance, it is recommended that TVS is not assembled by default)
The signal connection relationship between the module using the X65 platform and the QTM545/547 module is as follows: VREG_1P9(Pin 48) mmW ANT IFV4, mmW ANT IFH3, mmW Mod3_PON(Pin 44) connect to QTM U1. mmW ANT IFV2, mmW ANT IFH1, mmW Mod0_PON(Pin 40) connect to QTM U2. mmW Mod1_PON(Pin 42) is not used, please float. mmW Mod2_PON(Pin 46) is not used, please float.
The signal connection relationship between the module using the X55 platform and the QTM525 module is as follows: VREG_1P9(Pin 48) mmW ANT IFV4, mmW ANT IFH1, mmW Mod0_PON(Pin 40) connect to QTM U1. mmW ANT IFV1, mmW ANT IFH4, mmW Mod1_PON(Pin 42) connect to QTM U2. mmW ANT IFV3, mmW ANT IFH2, mmW Mod2_PON(Pin 44) connect to QTM U3. mmW ANT IFV2, mmW ANT IFH3, mmW Mod3_PON(Pin 46) connect to QTM U4.
The signal connection relationship between the module using the X55 platform and the QTM527 module is as follows: VREG_1P9(Pin 48) mmW ANT IFV4, mmW ANT IFH1, mmW Mod3_PON(Pin 46) connect to QTM U1. mmW ANT IFV3, mmW ANT IFH2, mmW Mod0_PON(Pin 40) connect to QTM U2. mmW ANT IFV2, mmW ANT IFH3, mmW Mod1_PON(Pin 42) connect to QTM U3. mmW ANT IFV1, mmW ANT IFH4, mmW Mod2_PON(Pin 44) connect to QTM U4.
QTM_THERM (Pin 61) is used for QTM module by default, and it is not recommended to use it for other purposes.
mmW Mod_VDD_IO(Pin 48) needs to add 4.7uF+22pF filter capacitor (mmW). The current of a single QTM module is greater than 0.2A, and the DC ESR of the power trace is less than 100m Ω . (Only one QTM545 module works at the same time)
VBAT needs to add 10uF+100pF filter capacitor (mmW). The current of a single QTM module is greater than 1.5A, and the DC ESR of the power trace is less than 80m Ω . (Only one QTM545 module works at the same time)
A 47uF~100uF capacitor is reserved near the main power supply pin of the QTM module to prevent voltage instability. It is not assembled by default.
The model of the board-to-board male connector used on the QTM545 module is AXG4B0612DJ1/818019183, and the model of the mated board-to-board female connector is AXG3B0612DJ1/818022986. Please pay attention to whether the model is selected correctly.

Check results (Tick <input checked="" type="checkbox"/> before <input type="checkbox"/>)			Notes
<input type="checkbox"/> YES	<input type="checkbox"/> NO	<input type="checkbox"/> NA	
<input type="checkbox"/> YES	<input type="checkbox"/> NO	<input type="checkbox"/> NA	
<input type="checkbox"/> YES	<input type="checkbox"/> NO	<input type="checkbox"/> NA	
<input type="checkbox"/> YES	<input type="checkbox"/> NO	<input type="checkbox"/> NA	
<input type="checkbox"/> YES	<input type="checkbox"/> NO	<input type="checkbox"/> NA	
<input type="checkbox"/> YES	<input type="checkbox"/> NO	<input type="checkbox"/> NA	
<input type="checkbox"/> YES	<input type="checkbox"/> NO	<input type="checkbox"/> NA	
<input type="checkbox"/> YES	<input type="checkbox"/> NO	<input type="checkbox"/> NA	
<input type="checkbox"/> YES	<input type="checkbox"/> NO	<input type="checkbox"/> NA	Modules using the X55 platform have no VIO_1V8 output.
<input type="checkbox"/> YES	<input type="checkbox"/> NO	<input type="checkbox"/> NA	
<input type="checkbox"/> YES	<input type="checkbox"/> NO	<input type="checkbox"/> NA	
<input type="checkbox"/> YES	<input type="checkbox"/> NO	<input type="checkbox"/> NA	The FULL_CARD_POWER_OFF of the module using the X55/315 platform requires an external pull-down resistor of 10K~100K. <div>  </div>
<input type="checkbox"/> YES	<input type="checkbox"/> NO	<input type="checkbox"/> NA	
<input type="checkbox"/> YES	<input type="checkbox"/> NO	<input type="checkbox"/> NA	
<input type="checkbox"/> YES	<input type="checkbox"/> NO	<input type="checkbox"/> NA	
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	

<input type="checkbox"/> YES	<input type="checkbox"/> NO	<input type="checkbox"/> NA	
<input type="checkbox"/> YES	<input type="checkbox"/> NO	<input type="checkbox"/> NA	
<input type="checkbox"/> YES	<input type="checkbox"/> NO	<input type="checkbox"/> NA	
<input type="checkbox"/> YES	<input type="checkbox"/> NO	<input type="checkbox"/> NA	
<input type="checkbox"/> YES	<input type="checkbox"/> NO	<input type="checkbox"/> NA	
<input type="checkbox"/> YES	<input type="checkbox"/> NO	<input type="checkbox"/> NA	
<input type="checkbox"/> YES	<input type="checkbox"/> NO	<input type="checkbox"/> NA	
<input type="checkbox"/> YES	<input type="checkbox"/> NO	<input type="checkbox"/> NA	The software of the standard version module does not support this function by default, and a special customized version is required to enable this function.
<input type="checkbox"/> YES	<input type="checkbox"/> NO	<input type="checkbox"/> NA	
<input type="checkbox"/> YES	<input type="checkbox"/> NO	<input type="checkbox"/> NA	
<input type="checkbox"/> YES	<input type="checkbox"/> NO	<input type="checkbox"/> NA	
<input type="checkbox"/> YES	<input type="checkbox"/> NO	<input type="checkbox"/> NA	
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	The PCIE of the standard version module supports 3.3V level, if the customer requires to support 1.8V level, a special customized version is required.
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	

3V3_AUX

VDD_EXT

<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	
<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	
<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	<p>The software of the standard version module does not support these functions by default, and a special customized version is required to enable these functions.</p> <p>These functions are I2S, I2C, TDD_SYNS multiplexing pins, and each pin can only support one function at the same time</p>
<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	
<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	
<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	
<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	
<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	
<input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>	
<input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>	

<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	<p>1. The coexistence signal pins of the module using the 315/X55 platform are Pin 65 and Pin 63. Pin 65 of the module using the 315/X55 platform is defined as WL_TX_EN. When WIFI is working, input a high level to turn off the LAA frequency band of the module. Pin 63 of the module using the 315/X55 platform is defined as LAA_TX_EN. When the LAA frequency band of the module is working, it outputs a high level and turns off the 5G LNA of the WIFI module.</p> <p>2. The coexistence signal pin of SIM8260C-M2/SIM8262E-M2/SIM8262A-M2 module is Pin 63. Pin 63 of the SIM8260C-M2 and SIM8262E-M2 modules is defined as N79_TO_WL_TX_EN. When the N79 frequency band of the module is working, it outputs a high level and turns off the 5G LNA of the WIFI module. Pin 63 of the SIM8262A-M2 module is defined as WL_TO_N79/LAA_TX_EN. When WIFI is working, input a high level to turn off the LAA and N79 frequency bands of the module.</p> <p>3. The coexistence signal pins of the SIM8260G-M2/SIM8380G-M2 module are Pin 59 and Pin 60. Pin 59 of the SIM8260G-M2 and SIM8380G-M2 modules is defined as N79_TO_WL_TX_EN. When the N79 frequency band of the module is working, it outputs a high level and turns off the 5G LNA of the WIFI module. Pin 60 of the SIM8260G-M2 and SIM8380G-M2</p>
<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	<p>These pins are located in the ZIF socket on the bottom of the module. The standard version module does not have this socket. To use these pins, a special customized version is required.</p>
<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	
<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	
<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	
<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	
<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	
<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	
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<input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>	

<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	
<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	
<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	Lenovo customized modules do not support I2S.
<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	
<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	
<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	
<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	
<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	The hardware of the standard version module using the X55/315 platform does not support SPI by default, and a special customized version is required to enable the SPI interface and VOIP function. Modules using the X65/X62 platform do not support SPI.
<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	
<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	
<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	
<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	The module using the X55/315 platform reserves an eSIM chip in the internal USIM2 interface, and the M.2 interface of the module supports dual USIM interfaces. SIM8262A-M2/SIM8262E-M2/SIM8260C-M2 modules do not reserve an eSIM chip inside, and the M.2 interface of the module supports dual USIM interfaces. SIM8260G-M2/SIM8380G-M2 modules reserve an eSIM chip inside, and the M.2 interface of the module only supports one USIM interface.
<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	
<input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>	
<input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>	
<input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>	
<input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>	

<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	Please refer to the Hardware Design Guide for more information.
<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	
<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	
<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	This feature is under development.
<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	
<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	
<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	
<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	The hardware of the standard version module does not support this function, and a special customized version is required to enable this function.
<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	This pin can be configured as GPS_1PPS, but it only supports one of TDD_SYNC_PPS and GPS_1PPS functions at the same time.
<input type="checkbox"/> YES <input type="checkbox"/> NO <input type="checkbox"/> NA	
<input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>	The hardware of the standard version module does not support this function, and a special customized version is required to enable this function.
<input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>	The hardware of the standard version module does not support this function, and a special customized version is required to enable this function.
<input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>	
<input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>	
<input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>	
<input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>	

<input type="checkbox"/> YES	<input type="checkbox"/> NO	<input type="checkbox"/> NA	
<input type="checkbox"/> YES	<input type="checkbox"/> NO	<input type="checkbox"/> NA	
<input type="checkbox"/> YES	<input type="checkbox"/> NO	<input type="checkbox"/> NA	
<input type="checkbox"/> YES	<input type="checkbox"/> NO	<input type="checkbox"/> NA	
<input type="checkbox"/> YES	<input type="checkbox"/> NO	<input type="checkbox"/> NA	
<input type="checkbox"/> YES	<input type="checkbox"/> NO	<input type="checkbox"/> NA	SIM8380G-M2 only supports dual mmW antennas.
<input type="checkbox"/> YES	<input type="checkbox"/> NO	<input type="checkbox"/> NA	
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	

No	Check Items
1	General inspection
2	VBAT (Pin2/4/70/72/74)
	VIO_1V8 (Pin 65)
3	FULL_CARD_ POWER_OFF# (Pin 6)
4	RESET# (Pin 67)

5	USB signal circuit
6	PCIE signal
7	W82/W80 interface
8	Audio circuit
9	SPI

10	I2C
11	TDD_SYNC_PPS
12	QTM_THERMAL
13	USIM card interface and circuit
14	GPIO signal
15	GND

16	RF circuit
17	Differential Signal

315/X55/X65/X62 Series 5G M.2 Module PCB Layout Check List

Detailed check contents
Confirm whether the PCB package of M.2 connector provided by SIMCom are used. If the customer designs the package by himself, make sure that the package is correct.
Avoid 90-degree routing, use 135-degree or smooth arc routing to reduce signal reflection.
For RF, USB, PCIE, RGMI and other signal impedance control, PCB is recommended to use at least 6-layer HDI stack-up structure.
Must check whether the customer's heat dissipation design measures meet the requirements of 5G modules. For example: 1.The module should be kept away from heat sources and heat-sensitive devices. 2.The motherboard directly below the module needs to expose copper, and no devices can be placed, so that a thermal pad can be placed between the module and the motherboard for module heat dissipation. For detailed design of heat dissipation, please refer to <SIMCom_Module_Thermal_Design_Guide>
The filter capacitors should be placed close to the VBAT pin, the smaller the closer to the pins, the power supply trace should first pass through the large capacitor, then pass through the small capacitor, and finally reach the VBAT pin of the module.
The VBAT power supply requires star route, which needs to be led out from the battery connector or the output capacitor end of the LDO/DC-DC power supply. (For example, 5G module and QTM545/547 and W82 etc,VBAT need star route)
VBAT is the module power input, and the trace width must be greater than 5mm. DC ESR as low as possible.
The VBAT parallel TVS should be placed close to the module pins, and the GND pin of the TVS must be directly connected to the GND main plane. The VBAT trace must pass through the pin of TVS first and then connect to the VBAT pin of the module.
VBAT traces should be kept away from sensitive signals, especially RF, Audio, USB, PCIE, CLK, SDIO, RGMII, SPMI, EBI, etc.
Note that the width of the GND trace on the VBAT main return path must also ensure sufficient overcurrent capability. It is recommended to use the GND plane and add enough vias when changing layers.
The VIO_1V8 trace should be connected to the module pin in series with a resistor and then connected to TVS in parallel before supplying power to the peripheral components.
In order to prevent the DC voltage drop from being too large, it is recommended that the trace width be greater than 0.25mm.
Pay attention to protecting the FULL_CARD_POWER_OFF# traces, and the following measures can be taken: be isolated with ground, avoid being parallel to other signal traces, keep away from the edge of the board, and avoid excessively long surface traces.
The FULL_CARD_POWER_OFF# trace should pass through the TVS before connecting to the module FULL_CARD_POWER_OFF# pin. If a key is used, the TVS is placed close to the key.
Pay attention to protecting the RESET# traces, and the following measures can be taken: be isolated with ground, avoid being parallel to other signal traces, keep away from the edge of the board, and avoid excessively long surface traces.
The RESET# trace should pass through the TVS before connecting to the module RESET# pin. If a key is used, the TVS is placed close to the key.
EMI suppression components (such as TVS, common mode inductor) should be placed close to the USB connector, and the traces should first pass through the TVS and then connect to the relevant USB pins of the module.
The edge rate of the USB signal is very fast, so keep away from sensitive signals such as RF, audio, and clock.

The USB connector should be far away from the RF antenna, especially the 2.4G antenna, and the two should be well isolated.
The USB_HS_DP/M traces must control 90 ohm differential impedance, and the difference between the lengths of the two traces in the differential pair should be less than 0.7mm. The trace length is less than 100mm, and the number of vias is less than 2. Avoid forked traces affecting USB speed and recognition.
The USB_SS_RX_P/M,USB_SS_TX_P/M traces must control 85 ohm differential impedance, and the difference between the lengths of the two traces in the differential pair should be less than 0.7mm. The trace length is less than 100mm, and the number of vias is less than 2. Avoid forked traces affecting USB speed and recognition.
The AC capacitor in series with USB_SS should be placed close to the output pin for signal integrity. The two AC capacitors connected in series on each differential pair should be parallel and placed symmetrically close together, otherwise it may affect signal integrity and cause EMI problems.
The trace distance between RX and TX of USB_SS, between USB_SS/HS and other signals should not be less than 4 times the trace width.
Differential signals should be routed on the inner layer as much as possible, be isolated with stiched ground on both sides and solid ground on the adjacent PCB layers from end-to-end.
The USB connector should be close to the module and the traces should be as short as possible.
All high-speed or sensitive signals should be kept away from PCIE traces to prevent interference by them.
The PETp/n0、PERp/n0、REFCLKP/N traces must control 85 ohm differential impedance, and the difference between the lengths of the two traces in the differential pair should be less than 0.5mm. The trace length is less than 150mm.
There is no need to control equal length between PETp/n0, PERp/n0 and REFCLKP/N.
The AC capacitor in series with PCIE should be placed close to the output pin for signal integrity. The two AC capacitors connected in series on each differential pair should be parallel and placed symmetrically close together, otherwise it may affect signal integrity and cause EMI problems.
The trace distance between each differential pair of PCIE and between other signal traces should not be less than 4 times the trace width.
Differential signals should be routed on the inner layer as much as possible, be isolated with stiched ground on both sides and solid ground on the adjacent PCB layers from end-to-end.
Under the premise of meeting the thermal design requirements, the WIFI module should be properly close to the 5G module, shorten the power trace of the WIFI module, and reduce the DC ESR and voltage drop of the module.
The VBAT trace width of the WIFI module should be greater than 1.5mm.
The capacitor (10uF+1uF+100nF) connected in parallel to WL_VDD_VM should be placed close to the WIFI module, and the trace width should be greater than 0.6mm.
The capacitor (10uF+1uF+100nF) connected in parallel to WL_VDD_VL should be placed close to the WIFI module, and the trace width should be greater than 2mm. The DC ESR of the trace should be less than 5mΩ.
The capacitor (10uF+1uF+100nF) connected in parallel to WL_VDD_VH should be placed close to the WIFI module, and the trace width should be greater than 0.6mm.
SLEEP_CLK is the sleep clock of the module. The trace should be routed on the inner layer as much as possible, be isolated with stiched ground on both sides. Keep away from sources of interference such as power supplies, RF and high-speed signals.
I2S/PCM signals should be routed in a group and on the inner layer as much as possible, be isolated with stiched ground on both sides. Keep away from sources of interference such as power supplies, RF and high-speed signals.
The I2S_MCLK trace should be routed on the inner layer as much as possible, be isolated with stiched ground on both sides. Keep away from sources of interference such as power supplies, RF and high-speed signals.
SPI signals should be routed in a group and be isolated with stiched ground on both sides as possible. Keep away from sources of interference such as power supplies, RF and high-speed signals.
The SPI_CLK trace should be routed on the inner layer as much as possible, be isolated with stiched ground on both sides. Keep away from sources of interference such as power supplies, RF and high-speed signals.

I2C signals should be isolated with stitched ground on both sides as much as possible. Keep away from sources of interference such as power supplies, RF and high-speed signals.
The TDD_SYNC_PPS trace should control 50 ohm single-ended impedance, which should be isolated with stitched ground on both sides. Keep away from sources of interference such as power supplies, RF and high-speed signals. The rising edge T_r is less than 3ns, the falling edge T_f is less than 5ns, and the trace length is less than 40mm.
The NTC resistor should be placed close to the object or area that needs temperature measurement. The NTC temperature detection signal is an analog signal, which should be routed on the inner layer and be isolated with stitched ground on both sides. Keep away from sources of interference such as power supplies, RF and high-speed signals. The NTC resistor avoid sharing the return path with the large current on the GND plane, and it should be directly connected to the ground of the module as much as possible.
All signals of USIM card interface should be routed on the inner layer and be isolated with stitched ground on both sides as much as possible. Avoid parallel routing with high current traces and high frequency signals.
The SIM_CLK signal of USIM card interface should be routed on the inner layer individually and be isolated with stitched ground on both sides as much as possible. Keep away from the edge of the board and other high current traces and high frequency signals, do not run parallel routing under the shield to avoid ESD and other problems.
The TVS should be placed close to the USIM card socket, and the traces pass through the TVS first and then connect to the module.
The power and signal of the USIM avoid sharing the return path with the large current on the GND plane.
Note that the area under the shrapnel of the USIM card socket should be cleared to prevent long-term wear and tear from causing a short circuit with the motherboard.
If GPIO is configured as an interface such as SPI, UART, I2C, I2S, etc., the traces should be routed in groups according to the interface to which the signal belongs. Each group of signals should be isolated with stitched ground on both sides, and the high-speed clock should be isolated separately.
The ground plane near and below the module should be complete, and the number of ground vias should be sufficient, especially under the high-power chip of the module.
The TVS should be connected to the main ground plane of the PCB as close as possible to reduce the grounding impedance as much as possible.
Make sure the main GND plane is not damaged and the connectivity is good.
Make sure there are enough ground vias on the path from the main GND layer to the main GND of the module.
The PCB directly below the module should expose copper according to the exposed copper position and area of the module, so that a thermal pad can be placed between the module and the motherboard for module heat dissipation.
GND (Pin71/73/3/5) is the ground return pin of VBAT. These pins should be placed with a large enough ground plane and enough vias to Ensure a low impedance return path.
ANT traces should control 50 ohm single-ended impedance.
Under the premise of ensuring the impedance requirement, the ANT trace should be as short and wide as possible, which can reduce the PCB insertion loss in the high frequency band.
ANT traces and antenna areas should be kept away from power, clock, audio and other interference sources and sensitive signals, and ensure sufficient isolation.
The distance between the ANT trace and GND should be kept at 2 times trace width, and the distance between the ANT trace and other signal traces should be kept at least 5 times trace width. Place GND vias on the ground traces or ground plane around the ANT trace at intervals of 1/10 the signal wavelength.
It is best not to change layers for ANT traces, because each hole will cause at least 15% signal reflection, resulting in impedance discontinuity.
It is best not to place any vias in the vertical projection area of the ANT trace on the reference ground plane, otherwise it will deteriorate the flatness of the reference ground plane and affect the impedance. If the ANT trace refers to the surface ground plane, and there is a GND pad of the device directly above, the solder paste after the component is soldered will affect the continuity of the ANT impedance.

The copper layer at least 450um below the ANT pin must be cleared to reduce the influence of the parasitic capacitance formed by the ANT pad and the reference ground plane on high-frequency signals
If ANT_CTRL0, ANT_CTRL1, RFFE0_DATA, and RFFE0_CLK are configured as RFFE3_CLK/RFFE3_DATA to control the antenna tuner, the traces should control the 50-ohm single-ended impedance and be isolated with stitched ground on both sides, away from power, high-speed, switch, audio and other signals. The distance between RFFE_DATA and RFFE_CLK traces should be at least 2.5 times trace width, and the length difference should not exceed 1mm. The distance between RFFE and other signal traces should be at least 2.5 times trace width. The capacitance of the RFFE_MIPi trace should be less than 50pF.
mmW intermediate frequency signal IFV and IFH traces must control 50 ohm single-ended impedance, and ensure the isolation of IF signal in design.
The IFV and IFH traces of the same QTM antenna module must control the length difference within 0.2mm.
In order to reduce PCB trace loss, under the premise of ensuring the impedance requirement, the trace width of IFH and IFV should be kept at least 10mil.
In order to ensure low trace loss of IFH and IFV (QTM545<6dB, QTM547<1.5dB), it is recommended to use low-loss coaxial cables or mmW special PCB boards.
The QTM antenna module has a large thermal power, so heat dissipation measures should be taken into consideration during design.
When designing, the isolation between QTM and GNSS, LTE, Sub-6 and other antennas should be considered, and the coexistence design should be considered.
Differential pairs should be routed in parallel as much as possible to ensure that the two traces are tightly coupled.
If the differential pair needs to control the equal length through serpentine routing, please route the serpentine wire at the fan-out end of the module or the connector end, do not wrap the serpentine wire in the middle of the routing, and try to ensure the equal length and equidistance requirements of the differential signals.
The test points, capacitors, resistors, TVS, and other components connected by the differential pair should be parallel and placed symmetrically close together to prevent impedance mismatch and EMI problems.
When the differential pair is connected to components such as test points, capacitors, resistors, TVS, and common mode inductors, avoid trace forks.
The differential pair should minimize the number of punching and layer changes, and the vias should be placed symmetrically.

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